Amendments to the Claims

1. (Previously Presented) A method for improved digital communications, comprising:

receiving a frame in a digital communications stream, the frame having a training portion and a data portion, wherein the data portion comprises an encoded symbol, the encoded symbol having a plurality of code words, wherein each code word has a plurality of chips;

slicing a chip from the encoded symbol;

removing interference from the sliced chip;

deriving a more accurate estimate for the sliced chip based on a correlation among the chips in the code word; and

determining an updated estimate of the encoded symbol based on the more accurate estimate for the sliced chip.

2. (Original) The method of claim 1, wherein the receiving step further comprises receiving the encoded symbol during the data portion of a frame.

3. (Canceled)

4. (Currently Amended) The method of claim 1, further comprising deriving more accurate sliced chip estimates for a subset of the plurality of chips in the code word, wherein at least fifty percent of the more accurate sliced chip estimates are based on the correlation among the chips in the code word.

5. (Previously Presented) The method of claim 1, further comprising:

providing the more accurate estimate for the sliced chip to a feedback filter; and

storing the more accurate estimate for the sliced chip in the feedback filter.

6. (Currently Amended) The method of claim 5, wherein the removing step further comprises combining an output of the feedback filter with ~~a portion of~~ the encoded symbol for improved performance in removing interference from the sliced chip.

7. (Currently Amended) The method of claim 5, wherein at least fifty percent of estimates stored in the feedback filter comprise more accurate estimates of ~~a~~ sliced chips from the encoded symbol.

8. (Canceled)

9. (Previously Presented) A system for improved digital communications, comprising:

a chip slicer for extracting a chip from a code word, the code word received as part of an encoded symbol in a digital communication stream, the chip slicer configured to determine an estimate of an identification of the chip based in part on a correlation to one or more chips in the code word;

a feed back filter configured to determine a noise component based in part on one or more chip identifications output from the chip slicer, the feedback filter having a plurality of content registers, each of the content registers configured to store a chip identification value; and

a chip combiner configured to derive a more accurate symbol estimate based on the noise component from the feed back filter, wherein the chip combiner provides improved symbol estimates to the chip slicer.

10. (Previously Presented) The system of claim 9, wherein one or more content registers are updated with more accurate chip identification values during decision directed updating.

11. (Previously Presented) The system of claim 10, wherein a majority of the plurality of content registers contain chip identification values determined based on correlation among chips in the code word.

12. (Previously Presented) The system of claim 9, wherein the feed back filter comprises a finite impulse response ("FIR") filter, and wherein the chip combiner subtracts out postcursor inter-symbol interference from a current chip slicer input signal.

13. (Currently Amended) The system of claim 9, wherein the chip combiner derives ~~a~~ the more accurate symbol estimate based on a correlation among the chips in the code word.

14. (Currently Amended) A receiver for use in a block coded digital communications system, comprising:

a preprocessor for carrying out signal processing tasks and for providing a feed forward filter with baseband samples;

the feed forward filter for processing the baseband samples and for sending a digital data stream to a chip slicer in combination with any signal added or subtracted by a chip

combiner, the chip slicer configured to determine an estimate of an identification of ~~the~~ a chip based in part on a correlation to one or more chips in a code word; and

a feedback filter for processing previous chip slicer outputs and derive a noise component, and provide the noise component to the chip combiner to subtract interference from the current input to the chip slicer.

15. (Original) The receiver of claim 14, wherein coefficients for the feed forward filter and the feedback filter are selected based on minimum mean square error (MMSE) criterion using either adaptive techniques or based on computations involving a channel estimate.

16. (Previously Presented) The receiver of claim 14, wherein the chip slicer is configured to extract a portion of the data stream that corresponds to a single chip.

17. (Previously Presented) The receiver of claim 14, wherein the feedback filter feeds the noise component back into the chip slicer by way of the chip combiner so that the noise component is subtracted from the next incoming signal from the feed forward filter before the next incoming signal is fed into the chip slicer.

18. (Previously Presented) A receiver for use in a block coded digital communications system, comprising:

means for receiving a frame in a digital communications stream, the frame having a training portion and a data portion, wherein the data portion comprises an encoded symbol, the encoded symbol having a plurality of code words, wherein each code word has a plurality of chips;

means for slicing a chip from the encoded symbol;

means for removing interference from the sliced chip;

means for deriving a more accurate estimate for the sliced chip based on a correlation among the chips in a code word; and

means for providing the more accurate symbol estimate as input to the means for slicing the chip.

19. (Currently Amended) The receiver of claim 18, wherein the means for slicing the chip from the encoded symbol further comprises a chip slicer for extracting a the chip from the code word.

20. (Previously Presented) The receiver of Claim 19, wherein the means for removing interference from the chip further comprising a feed back filter configured to determine a noise component based in part on one or more sliced chips, the feed back filter having a plurality of content registers.

21. (Currently Amended) The receiver of claim 20, wherein the means for deriving the more accurate symbol estimate for the sliced chip based on a correlation among the chips in the code word further comprises a chip combiner configured to derive ~~a~~ the more accurate symbol estimate for ~~a~~ the sliced chip, and wherein the chip combiner provides improved symbol estimates to the means for slicing the chip.

22. (Previously Presented) A method for improved digital communications, the method comprising:

receiving an encoded symbol stream having a plurality of code words, wherein each code word has a plurality of chips;

slicing a chip from the encoded symbol stream;

determining an identification of the sliced chip based in part on a correlation among the plurality of chips in the codeword;

determining a noise component based at least in part on the identification of the sliced chip; and

combining the noise estimate with a subsequent chip from the encoded symbol stream.

23. (Previously Presented) The method of claim 22, wherein the code words comprise complementary code keying code words.

24. (Previously Presented) The method of claim 22, further comprising updating at least one previously determined chip slice identification based on the identification of the sliced chip, and wherein determining the noise component is based in part on the updated at least one previously determined chip slice identification and the identification of the chip slice.

25. (Currently Amended) A system for improved digital communications, the system comprising:

a chip slicer configured to receive an encoded signal stream having a plurality of code words, wherein each code word has a plurality of chips, the chip slicer configured to extract a

chip slice from the encoded signal stream and identify a corresponding chip value based in part on a correlation ~~among at least a portion~~ with one of the plurality of chips of the code word;

a feedback filter configured to receive the corresponding chip value from the chip slicer and determine a noise component based in part on the corresponding chip value; and

a combiner configured to receive a digital communications stream at a first input, the noise component from the feedback filter at a second input, and configured to combine the digital communications stream with the noise component and output the encoded signal stream.

26. (Previously Presented) The system of claim 25, wherein the feedback filter comprises a plurality of content registers, and the chip slicer is configured to update at least one of the content registers based on the corresponding chip value.